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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,725	07/01/2003	Leonard Forbes	501268.01	5767

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,725	FORBES, LEONARD	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12 and 22-32* is/are allowed.

6)☒ Claim(s) *13 and 16-21* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/21/4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimoji (U.S. Patent No. 5,463,579).

In re claim 13, Shimoji (Fig. 1) discloses a semiconductor device, comprising:

An array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions (2, 3) and a common floating gate structure (5) that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance.

In re claim 19, Shimoji (Fig. 5) discloses the device of claim 13, wherein the array further comprises a drain line extending in a first direction and coupling second source/drain regions of the first and second FETs, and further wherein the first source/drain region of the first and second FET extend in a second direction that is perpendicular to the first direction.

In re claim 20, Shimoji discloses the device of claim 19, wherein the array further comprises a gate line that extends in the second direction.

3. Claims 13 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Ozawa (U.S. Patent No. 5,461,249).

In re claim 13, Ozawa (Figs. 1-3) discloses a semiconductor device, comprising:

An array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions (11, 12) and a common floating gate structure (7a) that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance.

In re claim 19, Ozawa discloses the device of claim 13, wherein the array further comprises a drain line extending in a first direction and coupling second source/drain regions of the first and second FETs, and further wherein the first source/drain region of the first and second FET extend in a second direction that is perpendicular to the first direction.

In re claim 20, Ozawa discloses the device of claim 19, wherein the array further comprises a gate line that extends in the second direction.

In re claim 21, Ozawa discloses the device of claim 20, further comprising a decoder (20, 21) coupled to each of the drain line, the source drain region (via the drain line) and the gate line.

> e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 13, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Guterman et al. (US 2004/0063283 A1).

In re claim 13, Guterman (Figs. 1A-1D) discloses a semiconductor device, comprising:

An array having memory cells for storing a desired logic state, each cell further comprising first and second adjacent field effect transistors (FETs) having respective source/drain regions (102, 103) and a common floating gate structure (107) that is spaced apart from the source/drain regions of the first FET by a first distance, and spaced apart from the source/drain regions of the second FET by a second distance, wherein the first distance is less than the second distance.

In re claim 16, Guterman discloses the device of claim 13, wherein the common floating gate structure is comprised of polysilicon (section [0052], lines 13-14).

In re claim 17, Guterman discloses the device of claim 13, wherein the second distance is approximately about two times the first distance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guterman et al. (as above).

In re claim 18, Guterman discloses the device of claim 13, but does not expressly disclose the empirical distance that the floating gate is spaced apart to one side. It would have been obvious to one having ordinary skill in the art at the time the invention was made to shift the floating gate a small distance, on the order of 30 angstroms, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F. 2c 272, 205 USPQ 215 (CCPA 1980).

Allowable Subject Matter

7. Claims 1-12 and 22-32 are allowed.

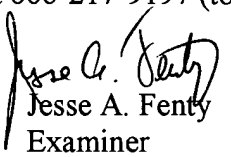
8. Claims 14 and 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jesse A. Fenty
Examiner
Art Unit 2815